New Design Method of Uniform and Nonuniform Distributed Power Amplifiers

Cedric Duperrier, Michel Campovecchio, Laurent Roussel, Monique Lajugie, and Raymond Quéré, *Senior Member, IEEE*

***Abstract*—A new design methodology of uniform and nonuniform distributed power amplifiers is reported in this paper. This method is based on analytical expressions of the optimum input and output artificial lines making up the uniform and nonuniform distributed architectures. These relationships are derived from the load-line requirement of each transistor size for optimum power operation. Furthermore, specific design criteria are presented to enable an efficient choice between uniform and nonuniform distributed architectures. To validate this new design methodology, a nonuniform distributed power amplifier has been manufactured at the TriQuint Semiconductor Foundry, Richardson, TX, using a 0.25-μm power pseudomorphic high electron-mobility process. This single-stage monolithic-microwave integrated-circuit amplifier is made of six nonuniform cells and demonstrates 1-W output power with 7-dB associated gain and 20% power-added efficiency over a multioctave bandwidth.**

***Index Terms*—Distributed amplifiers, design methodology, impedance matching, MMIC power amplifiers.**

I. Introduction

MONOLITHIC-microwave integrated-circuit (MMIC) power amplifiers are highly necessary for broad-band microwave communication systems and radars. Criteria such as maximum power and maximum efficiency, but also high reliability and high integration, are the most important issues.

The basic principle of distributed amplification overcomes the limitations related to finite gain-bandwidth product by paralleling devices so that their gate and drain capacitances are absorbed into artificial transmission lines. Unfortunately, several power-limiting mechanisms can be identified within distributed amplifiers [1], [2]. Indeed, each transistor demonstrates a strongly frequency-dependent power behavior so that the overall output power is only a small fraction of the combined power capabilities of all active devices [3], [4]. Distributed amplification has already demonstrated high performances for small-signal broad-band operation, but its power behavior must be carefully optimized using suited design methodologies.

A new design methodology based on nonuniform distributed power amplifiers is reported in Section III as a generalization of our previous work on uniform distributed power architectures [5]. The design parameters of artificial gate and drain lines are expressed as a function of the optimum power load of each FET size providing both the initial values and right directions in which the optimum tradeoff can be reached between wide-band and high-power operation.

Furthermore, Section III presents specific design criteria that enable to efficiently choose between uniform and nonuniform distributed architectures. Those design criteria are illustrated by the particular case of the MMIC nonuniform amplifier reported in Section IV.

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C. Duperrier and M. Campovecchio are with the Institut de Recherche en Communications Optiques et Microondes Laboratory, University of Limoges, 87060 Limoges, France (e-mail: cedric@ircom.unilim.fr).

L. Roussel and M. Lajugie are with the Thales Microwave Laboratory, 91349 Massy, France.

R. Quéré is with the Technology Institute of Electrical Engineering, 19100 Brive, France.

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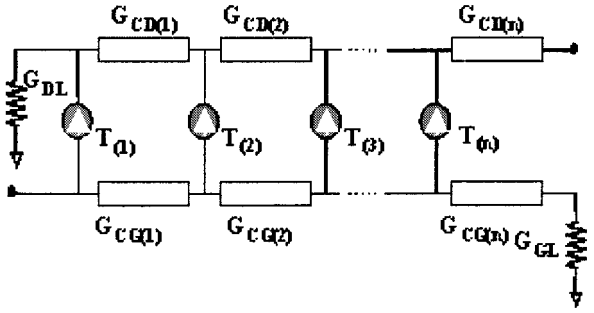

Fig. 1. Distributed power amplifier (n cells).

II. Design Methodology of Uniform Distributed Power Amplifiers

A distributed amplifier is called uniform if all transistors are identical. The design methodology of uniform power distributed amplifiers [5] is derived from the power matching conditions of each transistor and the equalization of their control voltages over the entire frequency band. It enables the analytical determination of artificial gate and drain-line characteristics as a function of the optimum power load required by each transistor.

Fig. 1 shows the general architecture of a distributed amplifier where the ith transistor is called $T_{(i)}(i = 1 \text{ to } n)$. The optimum characteristic conductances of gate and drain-line sections are, respectively, called $G_{\mathrm{CG}(i)}$ and $G_{\mathrm{CD}(i)}$, while the gate and drain dumping loads are, respectively, called G_{GL} and G_{DL}. It should be noted that the optimum input and output capacitances $(C_{\mathrm{IN}(i)}, C_{\mathrm{OPT}(i)})$ of each device are, respectively, absorbed into the artificial gate and drain lines to synthesize the optimum characteristic conductances $G_{\mathrm{CG}(i)}$ and $G_{\mathrm{CD}(i)}$.

A. Optimum Power Load

For power-amplifier design, one of the key points is the determination of the optimum input/output power loads that maximize the device output power $P_{\max}$ at 1-dB compression. The

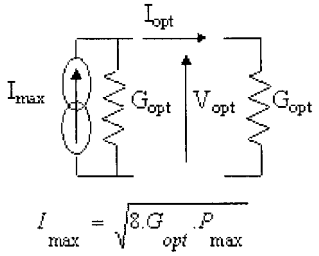

Fig. 2. Optimum power state of the device loaded by $G_{\rm opt}$.

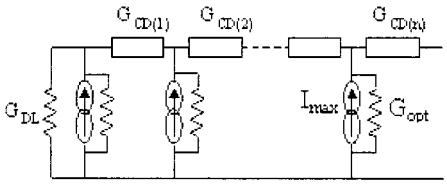

Fig. 3. Equivalent drain line for optimum design.

optimum power loads can either be determined by nonlinear simulations or by load–pull measurement [6]. As generally confirmed by experimental results on FETs, the conjugate of the optimum output power load is almost equivalent to a constant conductance $G_{\rm OPT}$ in parallel with a constant capacitance $C_{\rm OPT}$ over very wide bandwidths

$$Y_{\rm opt}(\omega) = G_{\rm opt} - j \cdot C_{\rm opt} \cdot \omega \quad \forall \omega \in [\omega_{\rm min}, \omega_{\rm max}]. \tag{1}$$

We have already demonstrated that the same conclusion on constant $(G_{\rm opt}, C_{\rm opt})$ is true for optimized cascode devices [7] so that the design methodology reported in this paper can be directly applied to cascode distributed amplifiers.

Therefore, the optimum power state of each transistor within a distributed amplifier requires equal control voltages and optimum power loads seen by each active device over the entire frequency band.

B. Drain-Line Design

In the particular case of uniform distributed amplifiers, the drain-line profile has to be synthesized for loading all devices with the same optimum output admittance $Y_{\rm opt}$.

Since the optimum output capacitance $C_{\rm opt}$ of each transistor is absorbed into the artificial drain line, the power optimization consists of loading the equivalent output generator of the transistor with the optimum power load $G_{\rm opt}$ (see Fig. 2). When transistor are replaced by their equivalent generator, the resulting drain line is shown in Fig. 3, where each drain section $G_{{\rm CD}(i)}$ must be synthesized to load each device generator $(I_{\rm max}, G_{\rm opt})$ by its optimum conductance $G_{\rm opt}$.

In the uniform case, assuming an identical gate voltage amplitude on each transistor (see Section II-C), the characteristic conductances $G_{{\rm CD}(i)}$ of the drain-line sections are given by

$$G_{{\rm CD}(1)} = G_{\rm opt} \tag{2}$$

$$G_{{\rm CD}(i)} = G_{\rm opt}\left(\frac{G_{\rm opt}}{G_{\rm opt}+G_{\rm DL}} + (i-1)\right), \qquad 2 \le i \le n. \tag{3}$$

The resulting optimum output power $P_{\rm out}$ of the uniform distributed amplifier is

$$P_{\rm out} = \left(\frac{G_{\rm opt}}{G_{\rm opt}+G_{\rm DL}} + (n-1)\right) \cdot P_{\rm max} \tag{4}$$

where n is the total number of transistors within the amplifier.

Indeed, for moderate bandwidth applications ($f_{\rm max}/f_{\rm min} < 3$), the amplifier output matching is not so critical, and we have already demonstrated that the dumping drain load $G_{\rm DL}$ may be suppressed [7]. Nevertheless, in order to consider the most general case of very large bandwidths, all equations take $G_{\rm DL} \neq 0$ since setting $G_{\rm DL} = 0$ in (3) and (4) enable to derive the optimum case for moderate bandwidths.

C. Gate-Line Design

In the same manner as in the drain-line case, the optimum characteristic conductances $G_{{\rm CG}(i)}$ of the gate line can be determined to match the equivalent input conductances $G_{{\rm IN}(i)}$ of transistors $T_{(i)}$ so that equal gate voltage amplitudes can be obtained over the frequency band. The equivalent input capacitances $C_{{\rm IN}(i)}$ are absorbed into gate-line sections to synthesize the optimum characteristic conductances $G_{{\rm CG}(i)}$ (see Fig. 1).

To achieve the equal gate voltage condition, the characteristic conductances $G_{{\rm CG}(i)}$ and the gate dumping load $G_{\rm GL}$ of uniform distributed amplifiers are given by

$$G_{{\rm CG}(i)} = \sum_{k=i}^{n} G_{\rm IN}(f_{\rm max}) \text{ and } G_{\rm GL} = G_{\rm IN}(f_{\rm max}). \tag{5}$$

It should be noted that the equivalent input conductances $G_{{\rm IN}(i)}$ are frequency dependent, which makes the gate matching accurate at a single frequency. However, when the characteristic conductances $G_{{\rm CG}(i)}$ are determined at the maximum operating frequency $f_{\rm max}$ (5), an almost constant gate voltage amplitude can be reached over wide frequency bands.

Moreover, in order to meet the condition of equal phase velocities on the gate and drain lines, the electrical lengths $\theta_{{\rm CG}(i)}$ and $\theta_{{\rm CD}(i)}$ of the corresponding artificial gate- and drain-line sections must verify

$$\theta_{{\rm CG}(i)} = \theta_{{\rm CD}(i)} \qquad \forall\, i = 1, \ldots, n. \tag{6}$$

D. New Design Criterion—Choice of Uniform and Nonuniform Distributed Power Amplifiers

In the case of uniform distributed amplifiers integrating identical transistors, the optimum power load $R_{\rm opt}$ is constant for each drain-line section. Fig. 4 shows the optimum characteristic impedances $Z_{{\rm CD}(i)}$ of each drain-line section calculated from (2) for three different values of $R_{\rm opt}$ (10, 100, 200 Ω)

$$R_{\rm opt} = 1/G_{\rm opt} \text{ and } Z_{{\rm CD}(i)} = 1/G_{{\rm CD}(i)}. \tag{7}$$

The equivalent optimum drain line (Fig. 3) shows that the design of a distributed power amplifier will be easier if the amplifier output is loaded by an impedance close to $Z_{{\rm CD}(n)}$ (usually inferior to 50 Ω).

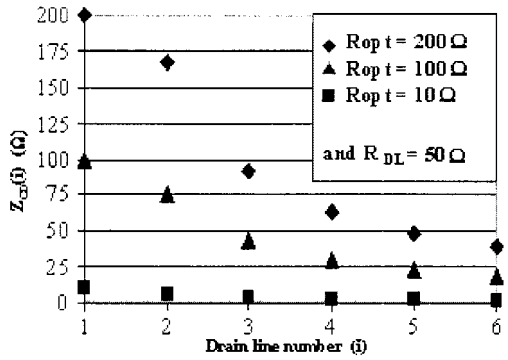

Fig. 4. Variation of the optimum characteristic impedances $Z_{\mathrm{CD}(i)}$ of each drain-line section for different optimum power loads R_{opt} (uniform distributed architecture).

Unfortunately, since most of the applications require a 50-Ω output load, it is very advantageous for the designer to choose the transistor size leading to a characteristic impedance $Z_{\mathrm{CD}(n)}$ as close as possible to 50 Ω. Therefore, looking at $Z_{\mathrm{CD}(6)}$ (see Fig. 4), it is clear that transistors having high R_{opt} (small size) are most interesting. In return, if the designer chooses a small size of transistor leading to a high R_{opt}, the first optimum drain-line section must synthesize a very high characteristic impedance $Z_{\mathrm{CD}(1)}$ (see Fig. 4). Finally, the difference between $Z_{\mathrm{CD}(1)}$ and $Z_{\mathrm{CD}(n)}$ is greatly increased so that the drain-line synthesis and matching are very difficult over wide bandwidths.

It is necessary to minimize the difference between $Z_{\mathrm{CD}(1)}$ and $Z_{\mathrm{CD}(n)}$ by using lower impedances R_{opt} (large size) for the first drain-line sections, while keeping high R_{opt} (small size) for the last sections. This conclusion has led us to implement nonuniform distributed architectures that enable to modify R_{opt} for each drain section by using different sizes of transistors.

III. Generalization to Nonuniform Distributed Power Amplifiers

A. Topology of the Nonuniform Distributed Amplifier

This section explains how using a nonuniform distributed architecture makes it possible to minimize the difference between $Z_{\mathrm{CD}(1)}$ and $Z_{\mathrm{CD}(n)}$ so that power matching is easier. Indeed, the optimum power load $R_{\mathrm{opt}(i)}$ can be increased with i by decreasing the transistor width $W(i)$ from i equals $1-n$.

In the case of nonuniform distributed amplifiers, each transistor $T(i)$ has a specific gatewidth $W(i)$. Therefore, the optimum power matching conditions $(G_{\mathrm{IN}}, G_{\mathrm{OPT}}, P_{\mathrm{max}})$, which were constant in the uniform case, now become $(G_{\mathrm{IN}(i)}, G_{\mathrm{OPT}(i)}, P_{\mathrm{max}(i)})$ and depend on the gatewidth $W(i)$ of the transistor $T(i)$.

B. Design Methodology

The new design methodology of nonuniform distributed power amplifiers is based on the same principle as for the uniform distributed architecture. At first, the optimum power loads $G_{\mathrm{IN}}(i)$ and $G_{\mathrm{OPT}}(i)$ are determined for each gatewidth $W(i)$ and the optimum characteristic conductances of gate- and drain-line sections are analytically expressed.

$\Rightarrow$ *Drain Line:* In the same manner as previously described for the uniform architecture, the characteristic conductances $G_{\mathrm{CD}(i)}$ can be successively determined. The first device $T_{(1)}$ provides a reduced output power $P_{OUT(1)}$ in comparison with its maximum output power capability $P_{\mathrm{max}(1)}$, but ensures that the other transistors $T_{(i\geq 2)}$ supply their maximum output power $P_{\mathrm{max}(i)}$. The generalized optimum power matching structure is analytically determined to add the individual power contributions in the direction of the output port

$$G_{\mathrm{CD}(1)} = G_{\mathrm{OPT}(1)} \tag{8}$$

$$G_{\mathrm{CD}(i\geq 2)} = \left(\frac{{G_{\mathrm{OPT}(1)}}^2}{G_{\mathrm{DL}} + G_{\mathrm{OPT}(1)}} + \sum_{k=2}^{i} G_{\mathrm{OPT}(k)} \right) \tag{9}$$

$$P_{OUT(1)} = \left(\frac{G_{\mathrm{OPT}(1)}}{G_{\mathrm{DL}} + G_{\mathrm{OPT}(1)}} \right) \cdot P_{\mathrm{max}(1)} \tag{10}$$

$$P_{\mathrm{OUT}} = P_{\mathrm{OUT}(1)} + \sum_{k=2}^{n} P_{\mathrm{max}(k)} \tag{11}$$

where $G_{\mathrm{CD}(i)}$ is the optimum characteristic conductance of the ith drain-line section, $P_{\mathrm{OUT}(1)}$ is the output power of the first device $T(1)$, P_{OUT} is the amplifier output power, $T(k)$ is the kth transistor with a gatewidth $W(k)$, $G\mathrm{opt}_{(k)}$ and $P\max_{(k)}$ are, respectively, the optimum output conductance and output power of the kth transistor $T_{(k)}$, and G_{DL} is the dumping drain load. Its value is chosen equal to $G_{\mathrm{CD}(1)}$.

It should be noted that, in the case of moderate bandwidth applications, the dumping load G_{DL} can be suppressed so that each transistor could be ideally power matched and yield its maximum output power. In this case, the optimum case becomes

$$G_{\mathrm{CD}(i)} = \sum_{k=1}^{i} G_{\mathrm{OPT}(k)} \text{ and } P_{\mathrm{OUT}} = \sum_{k=1}^{n} P_{\mathrm{max}(k)}. \tag{12}$$

Moreover, this new design methodology can be directly applied to nonuniform cascode distributed amplifiers since the conclusion of a constant $(G\mathrm{opt}, C\mathrm{opt})$ is true in the case of optimized cascode devices [7].

$\Rightarrow$ *Gate Line:* In the same manner as for the uniform case, gate-line sections are determined to match the input conductance $G_{\mathrm{IN}(i)}$ of each transistor $T_{(i)}$ so that equal gate voltage amplitudes could be obtained over the frequency band. To achieve the equal gate voltage condition, the characteristic conductances of gate-line sections are given by

$$G_{\mathrm{CG}(i)} = \sum_{k=i}^{n} G_{\mathrm{IN}_{(k)}} \quad G_{\mathrm{GL}} = G_{\mathrm{IN}(n)}. \tag{13}$$

Moreover, the electrical lengths $\theta_{\mathrm{CG}(i)}$ and $\theta_{\mathrm{CD}(i)}$ of the corresponding gate- and drain-line sections must always verify

$$\theta_{\mathrm{CG}(i)} = \theta_{\mathrm{CD}(i)}. \tag{14}$$

As a conclusion, depending on the optimum power load G_{opt} (mS/mm) of the device process and on the amplifier output load (50 Ω or less), improved output power performances can be achieved by using nonuniform distributed architectures with tapered gate and drain lines following the constraints (8)–(13). This new design methodology of nonuniform distributed power amplifiers represents a unified method since it includes the

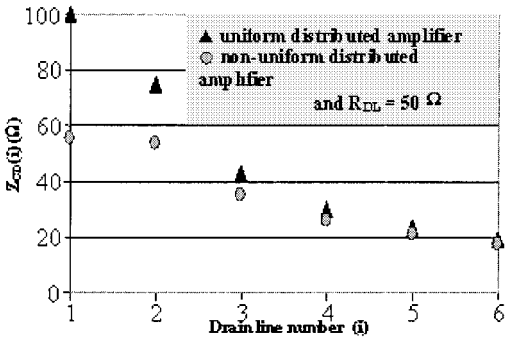

Fig. 5. Comparison of the optimum drain-line profiles between a uniform ($T_{(1\to6)} = 300\ \mu$m) and nonuniform amplifier ($T_{(1)} = 600\ \mu$m and $T_{(2\to6)} = 300\ \mu$m).

particular case of uniform architectures and enable to make an efficient choice between the two amplifier topologies. Indeed, taking $(G_{\mathrm{IN}(k)}, G_{\mathrm{opt}(k)}, P_{\mathrm{max}(k)})$ constant and equal to $(G_{\mathrm{IN}}, G_{\mathrm{opt}}, P_{\mathrm{max}})$ in (8)–(11), and (13) enable to retrieve (2)–(5) of the uniform case.

C. Comparison of Optimum Drain-Line Profiles for Uniform and Nonuniform Distributed Amplifiers

Section IV will report the design and measurement results of a nonuniform power distributed amplifier realized at the TriQuint Semiconductor Foundry, Richardson, TX, on its pseudomorphic high electron-mobility transistor (pHEMT) process. For this particular design, we now explain and illustrate why a nonuniform distributed amplifier has been chosen instead of a uniform architecture. The selected architecture integrates a 600-μm pHEMT as the first transistor $T(1)$, while the other transistors $T(i \geq 2)$ are identical 300 μm pHEMT.

Fig. 5 shows a comparison between the calculated optimum characteristic impedances $Z_{\mathrm{CD}(n)}$ of each drain-line section for two different topologies of the distributed amplifier as follows.

- A uniform distributed amplifier is calculated using (2) and (3) in the case of six identical 300-μm transistors ($R_{\mathrm{opt}(300\mu\mathrm{m})} = 100\ \Omega$).
- A nonuniform distributed amplifier is calculated using (8) and (9) in the case of a 600-μm device as first transistor ($R_{\mathrm{opt}(1)} = 56\ \Omega$) followed by five identical 300-μm devices ($R_{\mathrm{opt}(2\leq i\leq 6)} = 100\ \Omega$).

In the particular case of this pHEMT process, the nonuniform distributed amplifier has permitted to greatly minimize the difference between $Z_{\mathrm{CD}(1)}$ and $Z_{\mathrm{CD}(n)}$ ensuring an easier power matching design (see Fig. 5). Therefore, the nonuniform power distributed architecture has been selected since the uniform amplifier did not enable us to reach the specifications of 1-W output power up to 19 GHz.

IV. Application to a Single-Stage MMIC Amplifier

A nonuniform distributed power amplifier has been designed in cooperation with Thalès Laboratories, Massy, France, following this specific design procedure. The MMIC circuit has been manufactured using a 0.25-μm power pHEMT process from the TriQuint Semiconductor Foundry. The single-stage amplifier integrates six amplifying cells (see Fig. 6). The first

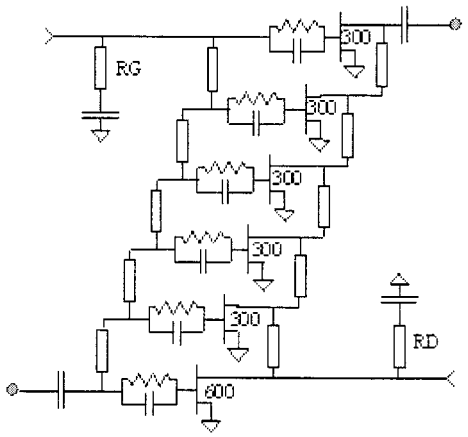

Fig. 6. Schematic of the nonuniform MMIC amplifier.

transistor $T(1)$ is a 600-μm pHEMT, while the other transistors $T(i \geq 2)$ are 300-μm pHEMTs. For this nonuniform architecture (see Fig. 6), (8) and (9), giving the optimum characteristic admittances $G_{\mathrm{CD}(i)}$ of the drain-line sections, can be simplified using the following assumptions:

$$G_{\mathrm{OPT}(1)} = G_{\mathrm{OPT}(600\,\mu\mathrm{m})} \approx 2 \cdot G_{\mathrm{OPT}(300\,\mu\mathrm{m})} \quad (15)$$

$$G_{\mathrm{OPT}(i\geq 2)} = G_{\mathrm{OPT}(300\,\mu\mathrm{m})}. \quad (16)$$

A. Nonlinear Modeling and Design Process

In a first step, the 300- and 600-μm devices have been modeled using pulsed I–V and pulsed S-parameter measurement. The optimum power loads provided by the foundry were then compared to nonlinear simulation results (a good agreement is obtained between the optimum power loads provided by the TriQuint Semiconductor Foundry and those obtained from simulation). Finally, the optimum power load of the 300- and 600-μm devices have been found sensibly constant up to 20 GHz and are equal to [$G_{\mathrm{OPT}(300\,\mu\mathrm{m})} = 10$ mS, $C_{\mathrm{OPT}(300\,\mu\mathrm{m})} = 0.18$ pF, $P_{\mathrm{max}} = 24$ dBm] and [$G_{\mathrm{OPT}(600\,\mu\mathrm{m})} = 18$ mS, $C_{\mathrm{OPT}(300\,\mu\mathrm{m})} = 0.31$ pF, $P_{\mathrm{max}} = 26.5$ dBm], respectively.

Uniform and nonuniform distributed amplifiers were initially designed and compared with the aim to supply 1-W output power and 20% power-added efficiency (PAE) over multioctave bandwidths. As previously explained (see Fig. 5), a nonuniform distributed architecture integrating a first device $T(1)$ of double gatewidth offered the best tradeoff between output power, gain, and return losses. Therefore, given the preceding optimum power loads $G_{\mathrm{OPT}(600\,\mu\mathrm{m})}$ and $G_{\mathrm{OPT}(300\,\mu\mathrm{m})}$, the tapered drain line has been optimized so that the first 600-μm device supplies a reduced output power (10), but enables the five following 300-μm devices to be almost ideally power matched. Fig. 7 shows the nonlinear simulation results for each device load line at f_{min} and f_{max}. In accordance with the preceding principle, it can be observed that the first device is affected by the dumping drain load G_{DL} and is not power matched, but enables the other devices to be almost ideally power matched.

The optimum tapered gate line has been obtained through a gate coupling capacitor profile along the input line. Discrete se-

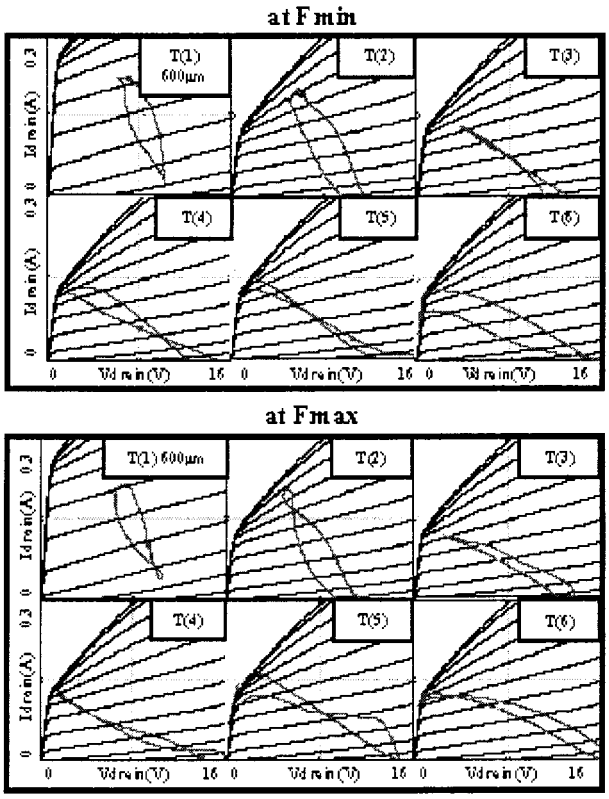

Fig. 7. Simulated device load lines at $f_{\min}$ and $f_{\max}$ ($T_{(1)} = 600\ \mu$m and $T_{(2\rightarrow 6)} = 300\ \mu$m).

ries capacitors couple each active device to the input line and act as voltage dividers to ensure equal drive levels on the transistor gates [8]–[10]. Implanted GaAs resistors shunt the series metal–insulator–metal (MIM) capacitors to supply gate bias.

B. Circuit Realization and Measured Performances

The nonuniform distributed power amplifier has been manufactured at the TriQuint MMIC Foundry, Richardson, TX, using a 100-μm-thick GaAs substrate and 0.25-μm power pHEMT. The main electrical parameters of this broad-band process are typically 295-mA/mm saturated current, -1-V pinchoff voltage and more than 16-V breakdown voltage for an associated power density of 800 mW/mm. The final circuit layout is shown in Fig. 8. It should be noted that the smallest values of gate coupling capacitances have been synthesized by two series capacitors in order to meet the minimum size constraint on MIM capacitors.

After wafer manufacturing, the nonuniform distributed amplifier was tested for dc operation and RF performances in class-A operation ($V\mathrm{ds} = 8$ V, $I\mathrm{ds} = 270$ mA). Fig. 9 shows a comparison between small-signal on-wafer measurements and simulations in the frequency band. A good agreement is obtained for input and output return losses that are lower than -10 dB in all of the bandwidth. The measured linear gain is 1 dB less than the simulated one and lies around 8.5 dB. At an input power of 23 dBm, on-wafer continuous-wave (CW) power measurements exhibited 30-dBm output power.

The exact cause of the rolloff observed at 18 GHz for the on-wafer measured gain (Fig. 9) is not known at this time. It seems that it is mainly due to the on-chip feature for the compensation of bonding wire effects at high frequency since bonding wires are not present under on-wafer conditions.

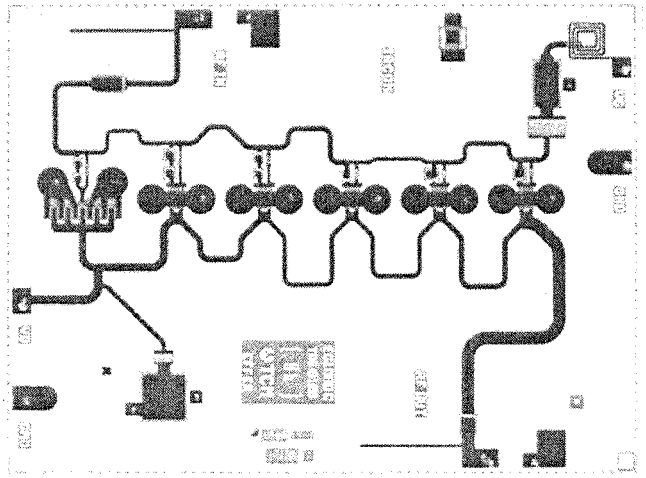

Fig. 8. Nonuniform MMIC distributed power amplifier.

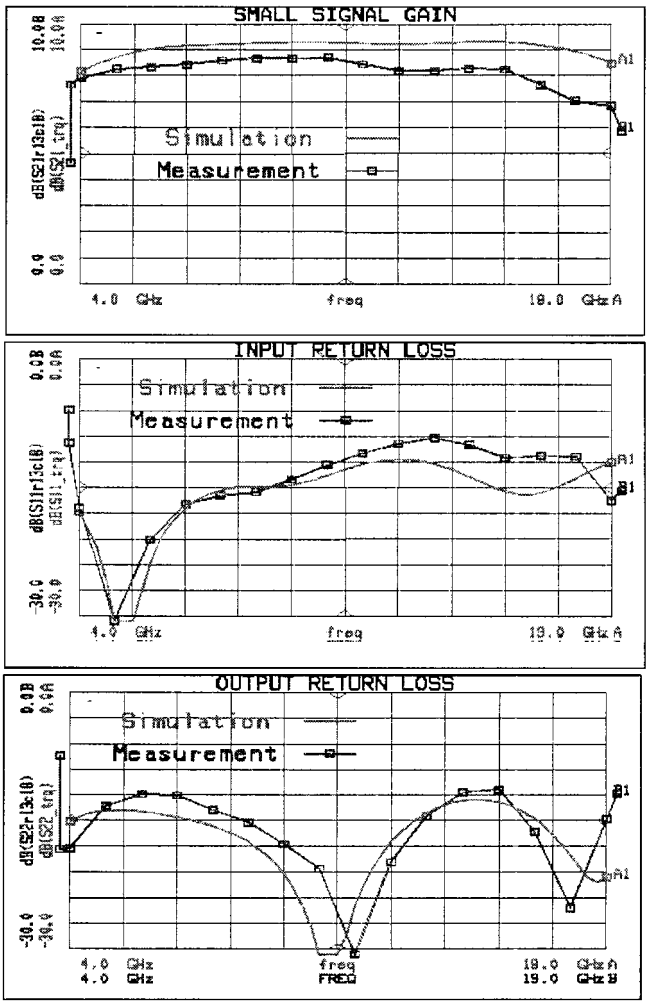

Fig. 9. Simulations and on-wafer measurements of small-signal gain and return losses.

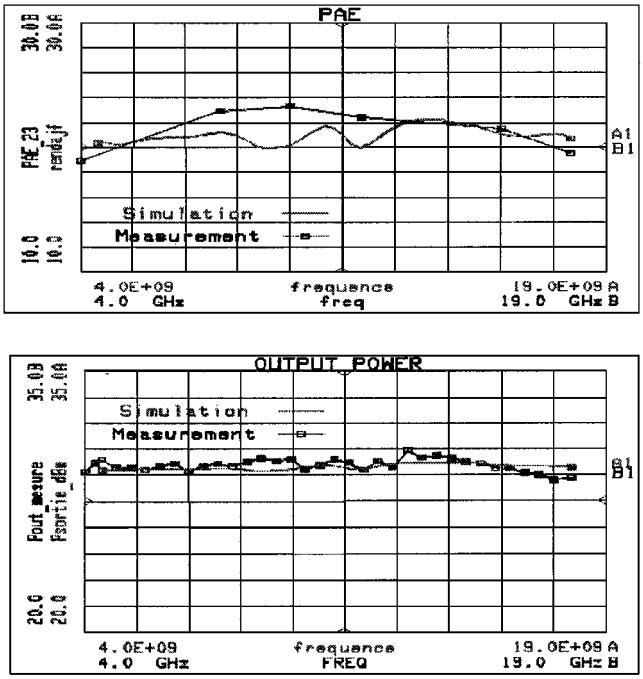

Fig. 10. Simulated and measured PAE and output power over the 4–19-GHz frequency band @$P\mathrm{in} = 23$ dBm, $V\mathrm{ds} = 8$ V and $I\mathrm{ds} = 270$ mA.

TABLE I
COMPARISON WITH RECENTLY PUBLISHED BROAD-BAND POWER AMPLIFIERS

Year	Stage	Trans.	Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	Ref
2000	1	PHEMT	2-8	35	20	9	[11]
2001	1	PHEMT	2-18	25	27	27	[12]
2001	1	HEMT	2-8	36	24	12	[13]

Test-fixture measurements have also been performed. The MMIC circuit was soldered on a molybdenum carrier and interfaced to the RF connectors with 13-mm-long 50-Ω microstrip alumina lines. The measured circuit exhibited 30-dBm CW output power and more than 20% PAE. Fig. 10 shows the good agreement obtained between predicted and measured output power and PAE up to 19 GHz.

All these results have been obtained after one foundry pass and without circuit tuning. For the sake of comparison, Table I presents performances obtained by three recently published broad-band power amplifiers.

V. CONCLUSION

A new design methodology of nonuniform distributed power amplifiers has been reported in this paper. This method is a generalization of our previous work on uniform distributed amplifiers [5]. It is based on analytical expressions of the optimum input and output artificial lines making up the nonuniform distributed architecture. These relationships are based on the optimum power load of each device size. Furthermore, given the optimum power load as a function of gatewidth, a design criterion has been presented that enables an efficient choice between uniform and nonuniform distributed topologies. To validate this specific methodology, a nonuniform single-stage distributed power amplifier has been designed and manufactured at the TriQuint Semiconductor Foundry, Richardson, TX, using a 0.25-μm pHEMT process. After one foundry pass, this MMIC amplifier demonstrated 1-W output power with 7-dB associated gain and a minimum of 20% PAE over a multioctave frequency band.

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Cedric Duperrier was born in Limoges, France, on June 25, 1974. He received the Post-Graduate Diploma in microwave communications from the University of Limoges, Limoges, France, in 1998, and is currently working toward the Doctor degree in electronic engineering at the University of Limoges.

Since 1998, he has been with the Institut de Recherche en Communications Optiques et Microondes (IRCOM) Laboratory, University of Limoges, where he is currently involved with distributed power amplifiers and microwave nonlinear circuit design.

Michel Campovecchio was born in Angers, France, in 1964. He received the Ph.D. degree in electronics from the University of Limoges, Limoges, France, in 1993.

In 1989, he was with the Thomson MMIC Foundry, Paris, France, where he was involved with FET nonlinear modeling. Since 1989, he has been with the Institut de Recherche en Communications Optiques et Microondes (IRCOM) Laboratory, University of Limoges. where he became an Associate Professor in 1994. His research interests include nonlinear circuit design and modeling, wide-band power amplifiers and high-speed amplifiers for 40 Gb/s optical communication (OC).

Laurent Roussel was born in Armentières, France, in 1965. He received the Electronic Engineering Degree from the University of Lille Flandres & Artois, Lille, France, in 1988.

He then joined Thomson-CSF, Paris, France, where he was involved in solid-state power-amplifier module design. He is currently with THALES Microwave, Massay, France, where he is involved in MMIC design for phased-array module.

Monique Lajugie, photograph and biography not available at time of publication.

Raymond Quéré (M'88–SM'99) received the Engineer and French Agregation degrees in applied physics from the Ecole National Supérieure d'Electrotechnique, Electronique, Informatique et Télécommunications (ENSEEIHT) Toulouse, Toulouse, France, in 1976 and 1978, respectively, and the Ph.D. degree from the University of Limoges, Limoges, France, in 1989.

In 1989, he became a Professor at the Technology Institute of Electrical Engineering (IUT), Brive, France, where he is involved in research concerned with nonlinear design and modeling of microwave circuits, with a special emphasis on nonlinear stability analysis of potentially unstable circuits such as oscillators, frequency dividers, and power amplifiers. He is also strongly involved with nonlinear characterization and modeling of microwave active devices based on pulsed measurements techniques.

Dr. Quéré is a member of the Technical Committee of the European Microwave Conference. He was a reviewer for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.